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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,780	07/24/2001	Taketoshi Nakano	70840-56281	3887

21874 7590 12/14/2005

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EXAMINER

LESPERANCE, JEAN E

ART UNIT	PAPER NUMBER
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2674

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/911,780

Applicant(s)

NAKANO ET AL.

Examiner

Jean E Lesperance

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

### DETAILED ACTION

1. The amendment filed on August 19, 2005 is entered and claims 1 to 8 are pending.
2. The objection of the drawings regarding Figures 5, 6 and 7 is withdrawn.
3. The rejection of claim 8 under 112, first and second paragraphs is withdrawn.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102 (b) as being unpatentable over U.S. Patent # 6,211,849 ("Sasaki et al.).

Regarding claim 1, Sasaki et al. teach a plurality of column electrode driving circuits Fig.2 (23) in a matrix type display device including a plurality of row electrode driving circuits Fig.2 (24) connected in series each for driving a plurality of row electrodes (24) and the plurality of column electrode driving circuits (23) connected in series each for driving a plurality of column electrodes,

each of the plurality of column electrode driving circuits (Fig.2 (23) comprising;  
a data input section (buffer amplifier, Fig.4 (4) for receiving a control data signal for the plurality of column electrodes (Fig.2 (23));

a timing control section (a control logic section Fig.4 (CT)) for generating a timing control signal for controlling at least one of the row electrode driving circuit (Fig.2 (24) and the column electrode driving circuit (Fig.2 (23);

a selection section for selecting one of a signal in synchronization with the timing signal generated by the timing control section and the control data signal input to the data input section, based on the control data signal input to the data input section (a control logic CT that includes a shift register circuit for sequentially selecting the predetermined number of signal lines by shifting (column 5, lines 12-15). In this case, the shift register is the selection section; and

a data output section for outputting one of the signal in synchronization with the timing signal and the control data signal which is selected by the selection section (second buffer amplifier for amplifying pixel data signal and the control signals output from the second latch circuit 7 (column 4, lines 67 and column 5, lines 1 and 2, see Fig.4 (8)), wherein the data input section (buffer amplifier, Fig.4 (4) of a second column electrode driving circuit of the plurality of column electrode driving circuits (Fig.2 (23) is connected to the data output section (Fig.4 (8) of a first column electrode driving circuit of the plurality of column electrode driving circuits Fig.2 (23) , and the data output section (Fig.4 (8) of the second column electrode driving circuit (Fig.2 (23) is connected to the data input section of a third column electrode driving circuit of the plurality of column electrode driving circuits (See how the column electrode driving circuits of Figure 3 are connected in series where the output of the first column electrode driving circuit is the input of the second column electrode driving circuit and the output of the

second column electrode driving circuit is the input of the third column electrode driving circuit (See also Figure 2)).

Regarding claim 2, Sasaki et al. teach the data input section (Fig.4 (4)) of the second column electrode driving circuit (Fig.2 (23)) includes an external data input port for receiving an external control data signal (CLK, DATA AND CNT, Fig.4 (2)) and a transferred data input port for receiving a control data signal from the first column electrode driving circuit, the external data input port and the transferred data input port being switchable (when the external data input receives the data, it switches the data to be transferred to the next port (see Figure 3)), and

the timing control section (a control logic section Fig.4 (CT)) of the second column electrode driving circuit is switchable to an operation state or a non-operation state in accordance with the switching between the external data input port and the transferred data input port (when the external data input receives the data, it switches the data to be transferred to the next port (See Figure 3)).

Regarding claim 3, Sasaki et al. teach the data input section Fig.3 (1) of the second column electrode driving circuit (Figure 4) receives one of the external data signal (the signals CLK, DATA and CNT Fig.4 (2)) and the control data signal (control logic Fig.4 (CT)) from the first column electrode driving circuit (Fig.3 (1)) which is selectively input thereto, and

the timing control section (a control logic section Fig.4 (CT)) of the second column electrode driving circuit (Fig.3 1) is switchable to an operation state or a non-

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operation state by the external control data signal (the signals CLK, DATA and CNT Fig.4 (2)).

Regarding claim 4, Sasaki et al. teach a display panel (liquid crystal panel Fig.2 (22);

a plurality of column electrode driving circuits on the display panel Fig.2 (23); and  
a plurality of row electrode driving circuits provided on the display panel Fig.2 (24),

wherein;

the plurality of column electrode driving circuits Fig.3 (1) are connected in series along a first side of the display panel, so that a scanning signal from the first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, is transferred in a cascading manner in the plurality of column electrode driving circuits (See how the column electrode driving circuits of Figure 3 are connected in series where the output of the first column electrode driving circuit is the input of the second column electrode driving circuit and the output of the second column electrode driving circuit is the input of the third column electrode driving circuit (See also Figure 2)),

the plurality of row electrode driving circuits Fig.2 (24) are connected in series along a second side of the display panel adjacent to the first side, so that the scanning signal from the first column electrode driving circuit is transferred in a cascading manner in the plurality of row electrode driving circuits (See how the row electrode driving circuits of Figure 3 are connected in series where the output of the first row electrode

driving circuit is the input of the second row electrode driving circuit and the output of the second row electrode driving circuit is the input of the third column electrode driving circuit (See also Figure 2)),

an external control data signal (CLK, DATA and CNT Fig.4 (2)) is input to the data input section Fig.4 (2) of the first column electrode driving circuit Fig.3 (1) and is output in synchronization with a timing signal generated by the timing control section (logic control Fig.4 (CT)) of the first column electrode driving circuit Fig.3 (1),

the external control data signal (CLK, DATA and CNT Fig.4 (3)) which is output from the first column electrode driving circuit Fig.3 (1) is transferred sequentially in the rest of the plurality of column electrode driving circuits in a cascading manner (see Figure 3), and

the timing signal is transferred sequentially in the plurality of row electrode driving circuits in a cascading manner as the scanning signal (Fig.4 (CT) where the timing control section is originated).

Regarding claim 5, Sasaki et al. teach a matrix type display device (a liquid display panel Fig.2 (22)), comprising:

a display panel Fig.2 (22);

a plurality of column electrode driving circuits connected in series and provided along a first side of the display panel Fig.2 (23); and

a plurality of row electrode driving circuits connected in series and provided along a second side of the display panel, the second side being adjacent to the first side (row electrode circuits connected in series, Fig.2 (24)).

wherein;

a control data signal for driving the display panel is input to a first column electrode driving circuit Fig.3 (1), among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits (the first column electrode circuit Fig.2 (23) is closest to a plurality of row electrode circuit (24),

a timing signal (logic control Fig.4 (CT)) for controlling an operation timing of the plurality of column electrode driving circuits (Fig.2 (23)) and the plurality of row electrode driving circuits Fig.2 (24) is generated in the first column electrode driving circuit Fig.2 (23), and the generated timing signal and a data signal are output to a second column electrode driving circuit, among the plurality of column electrode driving circuits, which is directly connected to the first column electrode driving circuit (see Fig.3),

the output data signal is transferred to a third column electrode driving circuit, among the plurality of column electrode driving circuits, which is directly connected to the second column electrode driving circuit (See how the column electrode driving circuits of Figure 3 are connected in series where the output of the first column electrode driving circuit is the input of the second column electrode driving circuit and the output of the second column electrode driving circuit is the input of the third column electrode driving circuit (See also Figure 2)), and

the generated timing signal is transferred in a cascading manner to the plurality of row electrode driving circuits as a scanning signal (See how the row electrode driving circuits of Figure 3 are connected in series where the output of the first row electrode



driving circuit is the input of the second row electrode driving circuit and the output of the second row electrode driving circuit is the input of the third column electrode driving circuit (See also Figure 2)).

Regarding claim 6, Sasaki et al. teach a matrix type display device (a liquid crystal panel having a matrix array of liquid crystal pixels (abstract)), comprising:

- a display panel Fig.2 (22);

- a plurality of column electrode driving circuits connected in series on a printed circuit board provided along a first side of the display panel (a plurality of column driving circuits are connected in series Fig.2 (23)); and

- a plurality of row electrode driving circuits connected in series and provided along a second side of the display panel, the second side being adjacent to the first side (a plurality of row electrode driving circuits are connected in series Fig.2 (24) which are adjacent to the column electrode driving circuits)),

wherein;

- each of the plurality of column electrode driving circuits is mounted in a tape carrier package (each of the plurality of column electrode driving circuits is mounted in a tape carrier package Fig.13 (9) interpreted as a array substrate);

- a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, generates a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits, generates a timing signal for controlling an operation timing of the plurality of column electrode

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driving circuits and the plurality of row electrode driving circuits, and outputs the generated timing signal to a first row electrode driving circuit, among the plurality of row electrode driving circuits, which is closest to the first column electrode driving circuit as a scanning signal (a first column electrode Fig.2 (23) which is closest to the row electrode driving circuit (see Fig.2 (24), a control logic section Fig.4 (CT) where the timing signal for controlling an operation timing is originated, a timing signal Fig.4 (CLK, DATA and CNT) is output from the column electrode driving circuit Fig.4 (1) by using different line portions as seen in Figure 13 (10) to the next column electrode driving circuit),

a timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially through a first line portion provided on the tape carrier package mounting the first column electrode driving circuit, a second line portion provided on the printed circuit board, a third line portion provided on the tape courier package mounting the first column electrode driving circuit, and a fourth line portion provided on the display panel (The waveforms of the pixel data signal and the control signals are shaped by the latch circuits 5 and 7, and that of the clock signal is shaped by the duty cycle regulator 6. In the latch circuits 5 and 7, the pixel data signal and the control signals are latched with reference to the timing of the clock signal, so as to recover the signals distorted during transmission. The duty cycle regulator 6 performs an operation of shaping the waveform of the clock signal, for example, while adjusting the threshold value thereof to trace the average value of the clock signal

voltage, and outputting the clock signal whose duty ratio is maintained at about 1:1 to the next driver IC 1 (column 5, lines 18-29)).

Regarding claim 7, Sasaki et al. teach a matrix type display device (a liquid crystal panel having a matrix array of liquid crystal pixels (abstract)), comprising:

- a display panel Fig.2 (22);

- a plurality of column electrode driving circuits connected in series on a printed circuit board provided along a first side of the display panel (a plurality of column driving circuits are connected in series Fig.2 (23); and

- a plurality of row electrode driving circuits connected in series and provided along a second side of the display panel, the second side being adjacent to the first side (a plurality of column driving circuits are connected in series Fig.2 (24)),

wherein a timing signal for controlling the plurality of row electrode driving circuits is supplied to one of the plurality of row electrode driving circuits sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel (a control logic section Fig.4 (CT) where the timing signal for controlling an operation timing is originated, a timing signal Fig.4 (CLK, DATA and CNT) is output from the column electrode driving circuit Fig.4 (1) by using different line portions as seen in Figure 13 (10) to the next column electrode driving circuit).

Regarding claim 8, Sasaki et al. teach a matrix type display device (a liquid crystal panel having a matrix array of liquid crystal pixels (abstract)), comprising

- a display panel Fig.2 (22);

a plurality of column electrode driving circuits connected in series on a circuit board provided along a first side of the display panel (a plurality of column driving circuits are connected in series on the circuit board Fig.2 (23)); and

a plurality of row electrode driving circuits connected in series and provided along a second side of the display panel, the second side being adjacent to the first side a plurality of row electrode driving circuits are connected in series Fig.2 (24) which are adjacent to the column electrode driving circuits,

Wherein;

a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, generates a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits, and outputs the generated timing signal to a first row electrode driving circuit, among the plurality of row electrode driving circuits, which is closest to the first column electrode driving circuit as a scanning signal (a first column electrode Fig.4 (1) which is closest to the row electrode driving circuit (see Fig.2 (23), a control logic section Fig.4 (CT) where the timing signal for controlling an operation timing is originated) and (See how the row electrode driving circuits of Figure 3 are connected in series where the output of the first row electrode driving circuit is the input of the second row electrode driving circuit and the output of the second row electrode driving circuit is the input of the third column electrode driving circuit (See also Figure 2)),

a timing signal generation circuit is provided to use for signals being different from a timing signal which is output from the first column electrode driving circuit and the timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially through the circuit board as not to be cross with the timing signal generation circuit (a timing signal Fig.4 (CLK, DATA and CNT) is output from the column electrode driving circuit Fig.4 (1) by using different line portions as seen in Figure 13 (10) to the next column electrode driving circuit . Given the broadest interpretation, the examiner assumes that the latch circuit Fig.4 (5) corresponding to the signal circuit).

#### ***Response to Amendment***

5. Applicant's arguments filed August 19, 2005 have been fully considered but they are not persuasive.

The applicant argued that the prior art does not teach "a selection section". Examiner disagrees with the applicant because the prior art teaches a control logic CT which includes a shift register circuit for sequentially selecting the predetermined number of signal lines by shifting (column 5, lines 12-15) corresponding to a selection section. In this case, the shift register is the selection section.

The applicant argued that the prior art does not teach "a control data signal that is input to a first column electrode driving circuit that is closest to the row electrode driving circuits". Examiner disagrees with the applicant because the prior art teaches the inter-module wirings 10 which are used to transmit the pixel data signal, clock signal

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and various control signals via each driver IC 1 (column 4, lines 34-36) corresponding to a control data signal that is input to a first column electrode driving circuit that is closest to the row electrode driving circuits and See the IC disposition of Fig.2.

The applicant argued that the prior art does not teach or suggest "a timing signal output from a first column electrode driving circuit that is supplied to a first row electrode driving circuit sequentially through a second line portion provided on a printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel". Examiner disagrees with the applicant because the prior art teaches a pixel data signal and the control signals are latched with reference to the timing of the clock signal, so as to recover the signals distorted during transmission (column 5, lines 21-24) where the timing signal travels by entering the first IC-1 input and to the output and so on through all the ICs (Fig.3) (see Fig.2, where the row and column electrodes are connected in a cascading manner where the timing travels from the first IC to the last IC).

The applicant argued that the prior art does not teach or suggest "a first column electrode that generates a timing signal for controlling a plurality of column electrode driving circuits and a plurality of row electrode driving circuits ". Examiner disagrees with the applicant because the prior art teaches a driving circuit for driving each of the scanning lines to select a row of the liquid crystal pixels and driving the signal lines to control voltages across the liquid crystal pixels of the selected row; wherein the driving circuit includes a signal line driver for sequentially driving the signal lines, and the signal line driver includes a plurality of driver ICs which are connected in cascade by inter-

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module wirings for transmitting at least a clock signal and a display signal and each of which sequentially supplies the display signal to a predetermined number of signal lines in synchronism with the clock signal, and each driver IC has a clock waveform shaping circuit for performing a clock signal waveform shaping by regulating a duty ratio of the clock signal to be output together with the display signal to a next stage (column 2, lines 36-50) (see Fig.2)). Looking at fig.2, all the IC are connected in a cascading manner where the timing signal controlling the first IC controlling also the last IC.

The applicant argued that the prior art does not teach "a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and a plurality of row electrode driving circuits is generated in the first column electrode driving circuit". Examiner disagrees with the applicant because the prior art teaches a driving circuit for driving each of the scanning lines to select a row of the liquid crystal pixels and driving the signal lines to control voltages across the liquid crystal pixels of the selected row; wherein the driving circuit includes a signal line driver for sequentially driving the signal lines, and the signal line driver includes a plurality of driver ICs which are connected in cascade by inter-module wirings for transmitting at least a clock signal and a display signal and each of which sequentially supplies the display signal to a predetermined number of signal lines in synchronism with the clock signal, and each driver IC has a clock waveform shaping circuit for performing a clock signal waveform shaping by regulating a duty ratio of the clock signal to be output together with the display signal to a next stage (column 2, lines 36-50) (see Fig.2)). Looking at fig.2, all

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the IC are connected in a cascading manner where the timing signal controlling the first IC controlling also the last IC.

### Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:00AM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

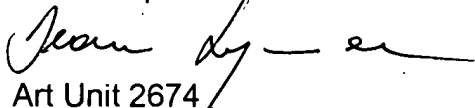
**or faxed to:**

(571) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance



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PATRICK N. EDOUARD  
SUPERVISORY PATENT EXAMINER